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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
03-2644 81693

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]

on _____

Signature _____

Typed or printed name _____

Application Number	Filed
10/828,408	04/19/2004

First Named Inventor
LAKSHMANAN, Viswanathan

Art Unit	Examiner
2825	Parihar, Suchin

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☑ attorney or agent of record. Registration number 38657.

☐ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 _____

/ Eric James Whitesell /
Signature

Eric J. Whitesell
Typed or printed name

760-720-0268
Telephone number

11/13/2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required.
Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	LAKSHMANAN, Viswanathan et al.
Serial No.:	10/828,408
Confirmation No. :	4517
Filed:	April 19, 2004
For:	METHOD AND COMPUTER PROGRAM FOR VERIFYING AN INCREMENTAL CHANGE TO AN INTEGRATED CIRCUIT DESIGN
Art Unit:	2825
Examiner:	Parihar, Suchin
Docket No.:	03-2644 81693

CERTIFICATE OF TRANSMISSION / MAILING

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November 13, 2006 / Eric James Whitesell /
Eric J. Whitesell #38657

BRIEF IN SUPPORT OF PRE-APPEAL REQUEST FOR REVIEW

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the final Office Action mailed on August 15, 2006 and the Advisory Action mailed on October 17, 2006, please enter the following brief in support of the attached Pre-appeal Request for Review. A Notice of Appeal is also submitted herewith.

ARGUMENTS

Morgan does not teach or suggest the claimed list of incremental changes

Claims 1 and 6 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Morgan, U.S. Patent 6,530,073 (Morgan) in view of Falbo, U.S. Patent Publication 2003/0163791 (Falbo). As explained in the specification on page 11, line 26 to page 12, line 2, the claimed list of incremental changes recited in Claims 1 and 6 includes all polygons added and all polygons deleted from the integrated circuit design by the engineering change order. In contrast to Claims 1 and 6, Morgan does not define incremental changes to the integrated circuit design in terms of adding and deleting polygons. In column 2, lines 50-55 cited in the advisory action, Morgan teaches adding and deleting cells. In contrast to Morgan, Claims 1 and 6 recite adding and deleting polygons. Polygons include features in an integrated circuit design that are not limited to cells. For example, the interconnects between cells are features in an integrated circuit design that include polygons apart from the cells. Accordingly, adding and deleting polygons does not require adding and deleting cells as alleged by the rejection. Because polygons may be added and deleted to an integrated circuit design without requiring the addition or deletion of cells, the addition and deletion of cells described in Morgan are not equivalent to the claimed adding and deleting polygons as alleged by the rejection. Because the addition and deletion of cells described in Morgan are not equivalent to the claimed adding and deleting polygons, Morgan does not teach or suggest the claimed list of incremental changes that includes all polygons added to the integrated circuit design and all polygons deleted from the integrated circuit design as alleged by the rejection.

Further, the incremental changes cited by the rejection in Morgan, column 11, lines 35-40, are not described as being included in a list of incremental changes. Consequently, Morgan does not teach or suggest the claimed list of incremental changes that includes all polygons added to the integrated circuit design and all polygons deleted from the integrated circuit design by the engineering change order. Because Morgan does not teach or suggest the claimed list of incremental changes that includes all polygons added to the integrated circuit

design and all polygons deleted from the integrated circuit design by the engineering change order, Morgan does not teach or suggest step (e) as alleged by the rejection. Because Morgan does not teach or suggest step (e), the modification of Morgan proposed by the rejection fails to arrive at the claimed invention. Because the modification of Morgan proposed by the rejection fails to arrive at the claimed invention, Claims 1 and 6 are not obvious under 35 U.S.C. § 103(a).

Sung does not teach translating the claimed marked integrated circuit design database to a file in generic data stream format

Claims 2 and 7 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Morgan in view of Falbo, and further in view of Sung, U.S. Patent Publication 2005/0216872 (Sung). Regarding Claims 2 and 7, the rejection errs in alleging that Sung teaches translating the claimed marked integrated circuit design database to a file in generic data stream format on page 4, paragraph [0044] and in FIG. 5. In contrast to Claims 2 and 7, Sung teaches generating a GDS file from a physical view that represents the cumulative reticle layers that form the semiconductor features on the integrated circuit. The advisory action errs in alleging that translating a netlist is equivalent to translating the claimed marked integrated circuit design database, because a netlist does not necessarily distinguish polygons that were changed from their current state as does the marked integrated circuit design database recited in independent Claims 1 and 6 from which Claims 2 and 7 depend. Because translating a netlist is not equivalent to translating the claimed marked integrated circuit design database, Sung does not teach or suggest translating the claimed marked integrated circuit design database. Because Sung does not translate the claimed marked integrated circuit design database to generate the GDS file, there is no basis for assuming that the resulting GDS file in Sung would be equivalent to the claimed file in generic data stream format. Because there is no basis for assuming that the resulting GDS file in Sung would be equivalent to the claimed file in generic data stream format, Sung does not teach or suggest translating the claimed marked integrated circuit design database to the claimed file in generic data stream format as alleged by the rejection. Because Sung does not teach or suggest translating the claimed marked integrated circuit design database to a file in

generic data stream format as alleged by the rejection, the modification of Morgan proposed by the rejection fails to arrive at the claimed invention. Because the modification of Morgan proposed by the rejection fails to arrive at the claimed invention, Claims 2 and 7 are not obvious under 35 U.S.C. § 103(a).

The fee for a notice of appeal is attached to this amendment.

Respectfully submitted,
/ Eric James Whitesell /
Eric J. Whitesell #38657

encl:

(1) pre-appeal request for review
(2) notice of appeal

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